In the Claims:

1. (Currently amended) An integrated circuit device, comprising:

a segmented CAM array **[[**that is**]]** configured to support a long word search operation as a plurality of overlapping segment-to-segment search operations that are each performed across different rows within a group of rows in the CAM array and staggered in time relative to one another.

2. (Currently amended) The device of Claim 1, wherein the plurality of overlapping segment-to-segment search operations includes a first segment-to-segment search operation **[[**that is**]]** performed in a first row in the group of rows and a second segment-to-segment search operation **[[**that is**]]** performed in a second row in the group of rows; and wherein commencement of the second segment-to-segment search operation is delayed in time relative to commencement of the first segment-to-segment search operation by one or two search segment time intervals.

3. (Original) The device of Claim 2, wherein upon commencement of the second segment-to-segment search operation, a precharged first match line segment in the first row is discharged in response to a leading edge of a force-to-miss control signal.

4. (Original) The device of Claim 2, wherein the second segment-to-segment search operation is preceded by the step of precharging a first match line segment in the second row while simultaneously discharging a corresponding first match line segment in the first row.

5. (Currently amended) The device of Claim 1, wherein a first row within the group of rows comprises:

first and second match line segments; and

a match line driver **[[**that is**]]** electrically coupled to the first match line segment and **[[**is**]]** responsive force-to-miss control signal.

6. (Original) The device of Claim 5, wherein the first row further comprises:

a match line signal repeater having an input electrically connected to the first match line segment and an output electrically connected to the second match line segment.

7. (Original) The device of Claim 5, wherein the first row further comprises:

a dual-capture match line signal repeater having an input electrically connected to the first match line segment and an output electrically connected to the second match line segment.

8. (Original) The device of Claim 5, wherein said match line driver is configured to electrically short the first match line segment to a ground reference potential in response to a leading edge of the force-to-miss control signal.

9. (Original) The device of Claim 8, wherein said match line driver is configured to precharge the first match line segment in response to a trailing edge of an evaluation control signal.

10. (Currently amended) An integrated circuit device, comprising:

a CAM array block having a segmented xN CAM array therein **[[**that is**]]** configured to support one-half of a x8N search operation as four overlapping segment-to-segment search operations that are performed in a staggered sequence across different rows within a quad group of rows in the CAM array.

11. (Currently amended) The device of Claim 10, wherein a first one of the quad group of rows comprises:

a first segment of CAM cells;

a first match line segment **[[**that is**]]** electrically connected to the first segment of CAM cells; and

a match line driver **[[**that is**]]** electrically connected to said first match line segment, said match line driver configured to precharge said first match line segment in response to an edge of a control signal and discharge said first match line segment in response to an edge of a force-to-miss control signal.

12. (Original) The device of Claim 10, wherein each of the rows in the quad group is responsive to a respective force-to-miss control signal.

13. (Currently amended) An integrated circuit device, comprising:

a CAM array having a segmented row of CAM cells therein that comprises:

first and second segments of CAM cells;

first and second match line segments **[[**that are**]]** electrically connected to said first and second segments of CAM cells, respectively;

a match line driver **[[**that is**]]** configured to precharge said first match line segment in response to an edge of a control signal and is responsive to a force-to-miss control signal; and

a dual-capture match line signal repeater having an input **[[**that is**]]** electrically coupled to said first match line segment and an output **[[**that is**]]** electrically coupled to said second match line segment.

14. (Original) The device of Claim 13, wherein said match line driver is configured to discharge said first match line segment in response to a leading edge of the force-to-miss control signal.

Claim 15 (Canceled).

16. (Currently amended) ~~The device of Claim 15,~~ An integrated circuit device, comprising:

a CAM array having a row of CAM cells therein, said row of CAM cells comprising:

first and second local word line drivers responsive to first and second local word line control signals, respectively, and ~~wherein the first and second local word line drivers are responsive to~~ a global word line control signal; and

first and second segments of CAM cells electrically coupled to the first and second local word line drivers, respectively.

17. (Currently amended) The device of Claim 16, wherein said CAM array has another row of CAM cells therein that comprises third and fourth local word line drivers, which are responsive to third and fourth local word line control signals, respectively, and third and fourth segments of CAM cells **[[**that are**]]** electrically coupled to the third and fourth word line drivers, respectively; and wherein the third and fourth local word line drivers are responsive to the same global word line control signal as the first and second local word line drivers.

18. (Currently amended) An integrated circuit device, comprising:

a CAM array having a row of lateral XY TCAM cells therein **[[**that are**]]** arranged in a repeating low-even, low-odd, high-even, high-odd sequence or a repeating high-even, high-odd, low-even, low-odd sequence.

19. (Currently amended) An integrated circuit device, comprising:

a segmented CAM array **[[**that is**]]** configured to support pipelined long word search operations in segment-to-segment and row-to-row search directions using a plurality of force-to-miss control signals to identify which rows are to be searched in the row-to-row pipeline direction.

20. (Original) A method of operating an integrated circuit device, comprising the step of:

staggering the timing of overlapping segment-to-segment search operations across different rows within a CAM array using force-to-miss control signals to establish miss conditions on match lines of rows that are not participating in respective ones of the segment-to-segment search operations.

Claims 21-56 (Canceled).